```
> D HIS
     (FILE 'USPAT' ENTERED AT 14:52:29 ON 18 SEP 94)
L1             1 S DIGITAL (5A) AUDIO (5A) LOGGER
L2           195 S DIGITAL (5A) (LOGGER OR LOGG?)
L3            11 S L2 AND AUDIO
L4             5 S L3 AND RAM
L5             1 S 4891835/PN AND MONITOR?
L6             1 S L5 AND BUFFER?
=>
```

The control **buffer** 222 provides several control signals to the components on the memory board 82. The control **buffer** 222 supplies a data strobe ("DS") signal to a board select or address decoder circuit 232. In addition, the control **buffer** 222 delivers an upper data strobe ("UDS") signal to a high column address strobe ("CAS") decoder 234 and a lower. . .

DETDESC:

DETD(50)

In . . . address into the address latches 220. Next, the CPU board 80 furnishes the data strobe ("DS") signal to the control **buffer** 222 through the control bus on the backplane. The control **buffer** 222 then delivers the data strobe signal to the board select circuit 232. This circuit determines if the DRAM on. . .

DETDESC:

DETD(51)

Assuming . . . timing circuit 256 delivers control signals to the high address multiplexer 238 and the low address multiplexer 240. The control **buffer** 222 delivers control signals to the high column address strobe decoder 234 and the low column address strobe decoder 236.. . .

DETDESC:

DETD(52)

The arbitration and timing circuit 256 then sends a data transfer acknowledge ("DTACK") signal to the control **buffer** 222, which supplies the DTACK signal to the CPU board 80 (FIG. 7) through the control bus on the backplane.. . .

DETDESC:

DETD(56)

The microprocessor 270 delivers data to and receives data from a data bus **buffer** 274 over a data bus 276. The data bus **buffer** 274 is connected to the data bus on the backplane. The microprocessor 270 delivers address signals to an address bus **buffer** 278 over an address bus 280. The address bus **buffer** 278 is connected to the address bus on the backplane. Furthermore, the microprocessor 270 delivers control signals to and receives control signals from a control bus **buffer** 282 over a control bus 284. The control bus **buffer** 282 is connected to the control bus on the backplane.

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=> D HIS
     (FILE 'USPAT' ENTERED AT 14:52:29 ON 18 SEP 94)
L1             1 S DIGITAL (5A) AUDIO (5A) LOGGER
L2           195 S DIGITAL (5A) (LOGGER OR LOGG?)
L3            11 S L2 AND AUDIO
L4             5 S L3 AND RAM
L5             1 S 4891835/PN AND MONITOR?
L6             1 S L5 AND BUFFER?
=>
```

> D L6 1 KWIC
US PAT NO: **4,891,835** [IMAGE AVAILABLE] L6: 1 of 1

DETDESC:

DETD(3)

Referring . . . another type of message channel, such as a radio channel. The telephone line 18 is one of the telephone lines **monitored** by the conventional magnetic tape logger 15. The message repeater 10 receives A.C. power through a power line 20.

DETDESC:

DETD(40)

The . . . CVSD encoder 176. The digital data from the register 178 is supplied through a data bus 180 to a data **buffer** 181. Then, the digital data is sent through the data bus on the backplane to the memory board 82 (FIG.. . .

DETDESC:

DETD(41)

FIG. . . . signals. Digital data is read from the memory and supplied through the data bus on the backplane to the data **buffer** 181. From the data **buffer** 181, the digital signals are supplied over the data bus 180 to a 16-bit parallel in/serial out register latch 182.. . .

DETDESC:

DETD(42)

Control . . . to the analog board 84 through the control bus on the backplane. The control signals are received by a control **buffer** 190. Similarly, address signals are supplied over the address bus on the backplane to an address **buffer** 192. The address **buffer** 192 then delivers the address signals to an address decoder 194. The control **buffer** 190 supplies control signals to the address decoder 194 and to a clock generator and timing control circuit 196. As. . .

DETDESC:

DETD(45)

FIG. . . . supplied over the address bus on the backplane to address latches 220 Similarly, control signals are supplied to a control **buffer** 222 through the control bus on the backplane. Data bus **buffers** 224 receive data from either the data bus on the backplane or the data bus 226 on the memory board. . . memory bank 228 and a low byte memory bank 230 supply data to and receive data from the data bus **buffers** 224 through the data bus 226.

DETDESC:

DETD(48)

> D L1 1

1. 5,339,203, Aug. 16, 1994, Apparatus and method of retrieving a message from a digital audio tape; John Henits, et al., 360/39, 32, 72.1 [IMAGE AVAILAB

=> D L4 1-5

1. 5,208,665, May 4, 1993, Presentation player for an interactive digital communication system; Karl W. McCalley, et al., 348/12; 455/5.1 [IMAGE AVAILABLE]

2. 5,195,092, Mar. 16, 1993, Interactive multimedia presentation & communication system; Steven D. Wilson, et al., 370/94.2; 340/825.5; 370/95.1, 110.1 [IMAGE AVAILABLE]

3. 5,191,410, Mar. 2, 1993, Interactive multimedia presentation and communications system; Karl W. McCalley, et al., 348/13; 379/105 [IMAGE AVAILABLE]

4. 5,113,496, May 12, 1992, Bus interconnection structure with redundancy linking plurality of groups of processors, with servers for each group mounted on chassis; Karl W. McCalley, et al., 395/200; 340/825.03, 827; 364/222.2, 222.3, 227.1, 228.3, 229, 229.5, 236.2, 237.2, 237.3, 237.8, 238, 238.3, 239, 239.8, 239.9, 240, 240.2, 241.9, 242.4, 242.94, 242.96, 248.1, 260, 260.2, 263.1, 268, 268.3, 268.7, 268.9, 271, 271.4, 282.1, 284, 284.2, 284.3, 919, 931.43, 940.68, DIG.1; 371/8.2, 11.2 [IMAGE AVAILABLE]

5. 4,891,835, Jan. 2, 1990, Method and device for recording and replaying **audio** communications; Keith K. W. Leung, et al., 379/88, 45, 51, 73 [IMAGE AVAILABLE]

=> D HIS

(FILE 'USPAT' ENTERED AT 14:52:29 ON 18 SEP 94)

L1 1 S DIGITAL (5A) AUDIO (5A) LOGGER
L2 195 S DIGITAL (5A) (LOGGER OR LOGG?)
L3 11 S L2 AND AUDIO
L4 5 S L3 AND RAM
=>
=>

=> D L7 1-5 KWIC

US PAT NO: 4,908,556 [IMAGE AVAILABLE] L7: 1 of 5

DETD(128)

Both data loggers 490 and 491 shown in FIGS. 10G and 10H, respectively, are controlled by a shared RAM "mailbox" interface. In addition, both are invoked in the servo interrupt routine immediately following the execution of the servo code.. . . is dictated by the servo update rate employed (currently this is 1 ms). In the case of the one-shot data logger , it can also be invoked via a subroutine call. This is provided so that conditions present during unexpected errors can. . .

DETD(129)

The shared RAM interface for the synchronous data logger is organized as follows (where all addresses are specified as offsets from a base address):

US PAT NO: 4,891,835 [IMAGE AVAILABLE] L12: 1 of 1

ABSTRACT:
A device according to the invention is compatible with conventional magnetic tape loggers. Such a device is termed a message repeater, and it records and replays audio signals forming messages on a. . .

BSUM(3)

Typically, a magnetic tape logger is a multi-channel, reel-to-reel tape recorder that is capable of concurrently recording signals from up to about forty channels. Police and fire departments, medical emergency services, public safety services, airlines, and trucking firms, among others, may employ a magnetic tape logger. Generally, the logger will be connected to a number of telephone lines and/or a number of radio channels so. . . messages may be recorded. The logger may operate continuously for twelve or more hours. Once the logger is stopped, the tape may be rewound to permit a particularly important message to be replayed.

BSUM(18)

In . . . are converted into corresponding digital signals, and the digital signals are stored in a storage device, such as a dynamic random - access memory ("DRAM") or other suitable storage device. Digital signals are selectively recalled from the memory, under operator control, and the recalled. . .

DETD(40)

The . . . CVSD encoder 176. The digital data from the register 178 is supplied through a data bus 180 to a data buffer 181. Then, the

digital data is sent through the data bus on the backplane to the memory board 82 (FIG.. . .

FIG. . . . supplied over the address bus on the backplane to address latches 220 Similarly, control signals are supplied to a control buffer 222 through the control bus on the backplane. Data bus buffers 224 receive data from either the data bus on. . .

DETD(48)

The control buffer 222 provides several control signals to the components on the memory board 82. The control buffer 222 supplies a data strobe ("DS") signal to a board select or address decoder circuit 232. In addition, the control buffer 222 delivers an upper data strobe ("UDS") signal to a high column address strobe ("CAS") decoder 234 and a lower. . .

ETD(57)

The . . . PROM 286 then delivers data to the data bus 276. In addition, the microprocessor 270 supplies address signals to a _random_ - _access_ _memory_ (" _RAM_ ") 288. The _RAM_ 288 is a scratch-pad memory. The _RAM_ 288 delivers data to the data bus 276. A clock generator 290 furnishes 16-MHz clock signals to the microprocessor 270,. . . 296 is connected to the address bus 280. The address decoder 296 provides selected signals to the PROM 286, the _RAM_ 288, the wait state generator 292, and the bus error generator 294.

=> D L1 1-7

1. 4,958,367, Sep. 18, 1990, Multichannel communications recorder having the capability to display channel activity and status; Raymond F. Freer, et al., 379/84; 360/22, 31 [IMAGE AVAILABLE]

2. 4,891,835, Jan. 2, 1990, Method and device for recording and replaying audio communications; Keith K. W. Leung, et al., 379/88, 45, 51, 73 [IMAGE AVAILABLE]

3. 4,888,652, Dec. 19, 1989, Communications recorder having a unique identification code and secure method and apparatus for changing same; Willy M. Sander, 360/5; 235/382.5; 340/825.31, 825.34 [IMAGE AVAILABLE]

4. 4,864,432, Sep. 5, 1989, Signal monitoring system with failsafe back-up capability; Raymond F. Freer, 360/27, 31, 53, 63; 369/47 [IMAGE AVAILABLE]

5. 4,851,937, Jul. 25, 1989, Apparatus for securing access to a communications recorder; Willy M. Sander, 360/69; 70/277; 340/825.31; 360/137 [IMAGE AVAILABLE]

6. 4,835,630, May 30, 1989, Modular configurable communications recorder; Raymond F. Freer, 360/69 [IMAGE AVAILABLE]

7. 4,827,461, May 2, 1989, Universal telecommunications audio coupling device; Willy M. Sander, 369/7; 360/67; 379/68 [IMAGE AVAILABLE]

=> D L7 1-5

1. 4,908,556, Mar. 13, 1990, Modular robot control system; Kenneth E. Daggett, et al., 318/568.2, 568.22; 395/84, 87, 96 [IMAGE AVAILABLE]

2. 4,868,474, Sep. 19, 1989, Multiprocessor position/velocity servo control for multiaxis _digital_ robot control system; Roy E. Lancraft, et al., 318/568.2, 562, 573; 395/84, 96; 901/19, 23 [IMAGE AVAILABLE]

3. 4,851,748, Jul. 25, 1989, Basic _digital_ multi-axis robot control having modular performance expansion capability; Kenneth E. Daggett, et al., 318/568.2; 395/84, 95, 96; 901/14, 23 [IMAGE AVAILABLE]

4. 4,786,847, Nov. 22, 1988, _Digital_ control for multiaxis robots;

Kenneth E. Daggett, et al., 318/568.2, 574; 395/84, 87, 93, 96, 97; 901/3, 23 [IMAGE AVAILABLE]

5. 4,763,055, Aug. 9, 1988, Digital robot control having high performance servo control system; Kenneth E. Daggett, et al., 318/568.14, 565, 567; 364/478; 395/80, 84, 95, 96; 901/25 [IMAGE AVAILABLE]

=> D L9 1-6

1. 4,958,367, Sep. 18, 1990, Multichannel communications recorder having the capability to display channel activity and status; Raymond F. Freer, et al., 379/84; 360/22, 31 [IMAGE AVAILABLE]

2. 4,891,835, Jan. 2, 1990, Method and device for recording and replaying audio communications; Keith K. W. Leung, et al., 379/88, 45, 51, 73 [IMAGE AVAILABLE]

3. 4,888,652, Dec. 19, 1989, Communications recorder having a unique identification code and secure method and apparatus for changing same; Willy M. Sander, 360/5; 235/382.5; 340/825.31, 825.34 [IMAGE AVAILABLE]

4. 4,864,432, Sep. 5, 1989, Signal monitoring system with failsafe back-up capability; Raymond F. Freer, 360/27, 31, 53, 63; 369/47 [IMAGE AVAILABLE]

5. 4,851,937, Jul. 25, 1989, Apparatus for securing access to a communications recorder; Willy M. Sander, 360/69; 70/277; 340/825.31; 360/137 [IMAGE AVAILABLE]

6. 4,835,630, May 30, 1989, Modular configurable communications recorder; Raymond F. Freer, 360/69 [IMAGE AVAILABLE]

=> D L12 1

1. 4,891,835, Jan. 2, 1990, Method and device for recording and replaying audio communications; Keith K. W. Leung, et al., 379/88, 45, 51, 73 [IMAGE AVAILABLE]

=> D HIS

(FILE 'USPAT' ENTERED AT 08:09:10 ON 08 MAR 94)

```
L1             7 S AUDIO (5A) LOGGER
L2        107521 S BUFFER
L3          1828 S DAT OR (DIGITAL AUDIO TAPE)
L4         68165 S RAM OR (RANDOM ACCESS MEMORY)
L5           297 S LOGGER AND (DIGITAL OR ANALOG)
L6            38 S AUDIO AND LOGGER
L7             5 S L2 AND L3 AND L4 AND L5
L8             0 S L1 AND L2 AND L3 AND L4
L9             6 S L1 AND L2
L10            0 S L9 AND L3
L11            6 S L9 AND (TAPE OR DISC)
L12            1 S L11 AND L4
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=> i

=> S L6 AND 360/CLAS

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         22418 360/CLAS
L13          7 L6 AND 360/CLAS
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=> D L13 1-7

1. 4,958,367, Sep. 18, 1990, Multichannel communications recorder having the capability to display channel activity and status; Raymond F. Freer, et al., 379/84; 360/22, 31 [IMAGE AVAILABLE]

2. 4,888,652, Dec. 19, 1989, Communications recorder having a unic identification code and secure method and apparatus for changing same; Willy M. Sander, 360/5 ; 235/382.5; 340/825.31, 825.34 [IMAGE AVAILABLE]

3. 4,864,432, Sep. 5, 1989, Signal monitoring system with failsafe back-up capability; Raymond F. Freer, 360/27 , 31 , 53 , 63 ; 369/47 [IMAGE AVAILABLE]

4. 4,851,937, Jul. 25, 1989, Apparatus for securing access to a communications recorder; Willy M. Sander, 360/69 ; 70/277; 340/825.31; 360/137 [IMAGE AVAILABLE]

5. 4,835,630, May 30, 1989, Modular configurable communications recorder; Raymond F. Freer, 360/69 [IMAGE AVAILABLE]

6. 4,827,461, May 2, 1989, Universal telecommunications audio coupling device; Willy M. Sander, 369/7; 360/67 ; 379/68 [IMAGE AVAILABLE]

7. 4,811,131, Mar. 7, 1989, Method and apparatus for scanning and recovering information from a record medium; Willy M. Sander, et al., 360/74.4 , 72.1 , 73.11 [IMAGE AVAILABLE]

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